USN | | | | | | | | | | |

14ELD151

First Semester M.Tech. Degree Examination, Dec.2015/Jan.2016
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. What is meant by "design methodology"? Explain different stages of design? **(08 Marks)**

b. Explain hardware/software codesign. **(04 Marks)**

c. Devise a one-hot code for the state of the traffic light. The possible states are RED, YELLOW and GREEN.
Develop a verilog model for a light controller that has encoded input, an encoded output and a single bit input that enables the lights. **(04 Marks)**

d. How does a parity bit enable detection of single bit errors? **(04 Marks)**

2 a. Develop a verilog model for a 7-segment decoder. Include an additional input, blank that overrides the BCD input and causes all segments not to be lit. **(10 Marks)**

b. Explain any two methods to improve the adder performance over that of a ripple-carry adder. **(10 Marks)**

3 a. Design a magnitude comparator to test for greater than inequality of two N-bit numbers. Give the verilog statement to satisfy the same. **(06 Marks)**

b. Design a data path to perform a complex multiplication of two complex numbers. Design a control sequence for this system. Assuming that real and imaginary parts of operands and product are represented in fixed point numbers, develop a verilog model for the data path. **(10 Marks)**

c. Briefly distinguish between Moore and Melay finite state machines. **(04 Marks)**

4 a. Design a 64 K × 8-bit composite memory using four 16 K × 8-bit components. **(10 Marks)**

b. Develop a verilog model of a dual-port 4 K × 16-bit flow through SSRAM. One port will allow data to be written and read, while the other port only allows data to be read. **(06 Marks)**

c. Compute 12-bit ECC word corresponding to the 8-bit data word 10011001. **(04 Marks)**

5 a. Explain the steps involved in integrated circuit manufacturing. **(08 Marks)**

b. Explain the internal organization of an FPGA. Explain logic blocks and I/O blocks with necessary diagrams. **(10 Marks)**

c. What are EMI and cross talk? **(02 Marks)**

6 a. Explain the instruction encoding for Gumnut instructions. **(10 Marks)**

b. Explain the organizations of cache memories. Explain the different techniques for cache data transfer. **(10 Marks)**

7 a. Give the verilog module that describes the I/O ports and the signals for connecting I/O ports. Show how to connect a 4×4 matrix keyboard controller to the defined ports. Give the verilog modules that shows the inter connections. **(12 Marks)**

b. Design an input controller that has 8 bit binary coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded core when the input value changes. The controller is the only interrupt source in the system. Develop the verilog model for the designed input controller. **(08 Marks)**

8 a. Explain the need for accelerators? Discuss the architectures of accelerators and issues of data transfer between a device and embedded systems memory. **(10 Marks)**

b. What is the necessity of BIST? Explain. How pseudo random patterns are generated and used for built in self test? **(10 Marks)**

* * * * *